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UNITED STATES PATENT APPLICATION

OF

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FOR

LIQUID CRYSTAL DISPLAY DEVICE

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[0001] This application claims the benefit of Korean Patent Application No. 2002-88203, filed on December 31, 2002, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a liquid crystal display, and more particularly to a liquid crystal display that is adaptive for improving picture quality by eliminating residual DC components within a horizontal electric field type liquid crystal display panel.

Discussion of the Related Art

[0003] Generally, liquid crystal display devices display a natural-like motion picture using thin film transistors TFT as switching devices. Such liquid crystal display devices can be made small-sized in comparison to cathode ray tubes CRT and have been commercialized as potable televisions, notebook computers and the monitors of personal computers.

[0004] The liquid crystal display device displays pictures corresponding to video signals like television signals in a pixel matrix or picture element matrix where pixels are arranged at each crossing area of gate lines and data lines. Each pixel includes a liquid crystal cell that controls the amount of transmitted light in accordance with the voltage level of a data signal. The TFT is installed at the crossing area of the gate line and the data line and switches the data signal, which is to be transmitted to the liquid crystal cell, in response to a scan signal, i.e., gate pulse, from the gate line.

[0005] Such liquid crystal display device can be classified into a vertical electric field type liquid crystal display device and a horizontal electric field type liquid crystal display device in accordance with the direction of electric field by which liquid crystal is driven, wherein the vertical electric field type liquid crystal display device has an electric field of vertical direction applied and the horizontal electric field type liquid crystal display device has an electric field of horizontal direction applied and a viewing angle widened.

[0006] The horizontal electric field type liquid crystal display device, differently from the vertical electric field type liquid crystal display device, has the liquid crystal within a pixel cell rotate on the basis of the horizontal direction by the horizontal electric field, thus there is an advantage that the viewing angle is wide.

[0007] FIG. 1 is a diagram representing a signal line of a horizontal electric field type liquid crystal display device of the related art.

[0008] Referring to FIG. 1, a lower substrate 2 provided with a TFT array includes a plurality of common lines CL1 to CLm to apply common voltages Vcom to common electrodes, a plurality of gate lines GL1 to GLm to apply gate voltages to gate electrodes, and a plurality of data lines DL1 to DLn to apply data voltages to pixel electrodes.

[0009] The common lines CL1 to CLm are a number m of lines formed parallel to the gate lines GL1 to GLm.

[0010] The gate lines GL1 to GLm are a number m of lines formed alternate with and parallel to the common lines CL1 to CLm and apply the gate voltages to the gate electrodes of the TFTs.

[0011] The data lines DL1 to DLn are a number n of lines formed perpendicularly to the gate lines GL1 to GLm. The data lines DL1 to DLn apply data signals to pixel electrodes through the drain electrodes of the TFTs. Pixel areas are formed at the intersection area of the common line CL and the gate line GL that cross the data line DL. Thin film transistors are also formed at the crossing area of the data line DL and the gate line GL.

[0012] Supply lines SL are formed at both sides of the lower substrate 2 in a perpendicular direction at least to the gate lines GL1 to GLm. The supply lines SL apply common voltages to the common line CL. A static electricity prevention circuit 4 and 8 is installed between the supply line SL and signal lines including the gate line GL, the data line DL and the common line CL.

[0013] The gate lines GL1 to GLm and the data lines DL1 to DLn of the horizontal electric field type liquid crystal display device of the related art are frequently broken because of manufacturing tolerance and operational error. When the gate line GL1 to GLm is broken, some of the TFTs are not driven. When the data line DL1 to DLn is broken, the data signal is not applied to some of the TFTs. To determine if there are broken lines in the gate lines GL1 to GLm and the data lines DL1 to DLn, the TFT array substrate is inspected with a test circuit (not illustrated). After completing the test, a residual DC component within the liquid crystal display panel is bypassed through the supply line SL to be eliminated.

[0014] On the other hand, whether the TFT runs normal or not is detected with an output voltage value obtained by applying voltage to each of a gate shorting bar 12 and a data shorting bar 10 in order to test the operation of the TFT.

[0015] The gate shorting bar 12 is connected to at least any one of the gate lines GL and the common lines CL, and the data shorting bar 10 is connected to the data DL. At least any one of the gate line GL and the common line GL connected to the gate shorting bar 12 is connected to the supply line SL through a static electricity prevention circuit 4 and the data line DL connected to the data shorting bar 10 is connected to the supply line SL through the static electricity prevention circuit 4. The supply line SL surrounds the display area of the lower substrate 2 and is connected to the static electricity prevention circuit 4 and 8 that is formed at both ends of each of the data line DL, the gate line GL and the common line CL.

[0016] In this way, the related art liquid crystal display panel has a bypass loop formed through the supply line SL. A DC component and a power off signal remaining within the liquid crystal display panel is bypassed through the bypass loop and naturally discharged.

[0017] However, if there is poor a contact between the bypass loop and the signal lines or if there is a defect in the bypass loop, the remaining DC component is applied to the display area of the liquid crystal display panel causing contaminant within the liquid crystal display panel to be excited, thereby deteriorating picture quality in the display area. Specifically, stains appear particularly around a liquid crystal injection hole (not shown), thus the picture quality is deteriorated.

SUMMARY OF THE INVENTION

[0018] Accordingly, the present invention is directed to a liquid crystal display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0019] Accordingly, it is an advantage of the present invention to provide a liquid crystal display that is adaptive for improving picture quality by eliminating residual DC components within a horizontal electric field type liquid crystal display panel.

[0020] In order to achieve these and other advantages of the invention, a liquid crystal display device according to an aspect of the present invention includes a substrate defined as a display part and a non-display part; a gate line formed on the substrate; a common line formed parallel to the gate line; a data line crossing the gate line and the common line while being insulated, to determine a pixel area; and at least one capacitor located in the non-display part and connected to at least one of the gate line, the common line and the data line for storing up a remaining component of the display part and eliminating the stored component.

[0021] The liquid crystal display device further includes a common electrode formed in the display part of the substrate and connected to the common line; a thin film transistor formed at an intersection area of the gate line and the data line; a gate insulating film formed between the gate line and the data line; a protective film formed on the gate insulating film for protecting the thin film transistor; and a pixel electrode connected to the thin film transistor to form a horizontal electric field with the common electrode.

[0022] The capacitor includes a first capacitor connected to at least one of the gate line and the common line; and a second capacitor connected to the data line.

[0023] The liquid crystal display device further includes a first static electricity prevention means formed in the non-display part of the substrate and connected to the first

capacitor; and a second static electricity prevention means formed in the non-display part of the substrate and connected to the second capacitor.

[0024] The first capacitor includes a first shorting bar connected to the first static electricity prevention means; at least one layer of insulating film formed on the first shorting bar; and a first dummy line formed to overlap the first shorting bar on the at least one layer of insulating film.

[0025] Herein, the first shorting bar is formed of the same metal as any one of the gate line and the data line.

[0026] Herein, the first dummy line is formed of the same metal as the pixel electrode.

[0027] Herein, the at least one layer of insulating film is the gate insulating film and the protective film.

[0028] Herein, the at least one layer of insulating film is the protective film.

[0029] The second capacitor includes a second shorting bar connected to the second static electricity prevention means; at least one layer of insulating film formed on the second shorting bar; and a second dummy line formed to overlap the second shorting bar on the at least one layer of insulating film.

[0030] Herein, the second shorting bar is formed of the same metal as any one of the gate line and the data line.

[0031] Herein, the second dummy line is formed of the same metal as the pixel electrode.

[0032] Herein, the at least one layer of insulating film is the gate insulating film and the protective film.

[0033] Herein, the at least one layer of insulating film is the protective film.

[0034] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute apart of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0036] In the drawings:

[0037] FIG. 1 a plan view representing a horizontal electric field type liquid crystal display device of the related art;

[0038] FIG. 2 is a plan view representing a horizontal electric field type liquid crystal display device according to the present invention;

[0039] FIG. 3 is a plan view representing a pixel illustrated in FIG. 2 and formed at a crossing area of a gate line and a data line on a lower substrate;

[0040] FIG. 4 is a sectional view representing the pixel taken along the line I-I' illustrated in FIG. 3;

[0041] FIG. 5 is a sectional view representing the pixel illustrated in FIG. 2 on an upper substrate; and

[0042] FIGs. 6A and 6B are sectional views representing first and second bypass capacitors illustrated in FIG. 2.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

[0043] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0044] FIG. 2 is a plan view representing a liquid crystal display device of In Plane Switching (IPS) mode according to the present invention.

[0045] Referring to FIG. 2, the liquid crystal display device of IPS mode according to the present invention includes a plurality of common lines CL1 to CLm to apply common voltages Vcom to common electrodes, a plurality of gate lines GL1 to GLm to apply gate voltages to the gate electrodes of TFTs, a plurality of data lines DL1 to DLn to apply data voltages to pixel electrodes through the drain electrodes of the TFTs, a first bypass capacitor C1 formed at an end of the data line DL1 to DLn, and a second bypass capacitor C2 formed at an end of the gate line GL1 to GLm. Herein, the common line CL, the gate line GL and the data line DL are formed in a display part 62, and the first and second bypass capacitors C1 and C2 are formed in a non-display part that does not include the display part 62.

[0046] The common lines CL1 to CLm are a number m of lines formed substantially parallel to the gate lines GL1 to GLm. Supply lines SL for applying a common voltage to the common lines CL1 to CLm are formed on both sides of a lower substrate 32 in a direction

substantially perpendicular to the gate lines GL1 to GLm. The common lines CL are directly connected to a second shorting bar 42 or connected a third static electricity prevention circuit that is in connection with the second shorting bar 42.

[0047] The gate lines GL1 to GLm are a number m of lines formed alternate with and substantially parallel to the common lines CL1 to CLm and applies the gate voltages to the gate electrodes of the TFTs. The gate lines GL are connected to the third static electricity prevention circuit 38 respectively, or connected to the second shorting bar 42 directly.

[0048] The data lines DL1 to DLn are a number n of lines formed substantially perpendicular to the gate lines GL1 to GLm and apply data signals to pixel electrodes through the drain electrodes of the TFTs. Among the data lines DL, odd-numbered data lines DL1, DL3, ..., DL(n-3), DL (n-1) are connected to a first shorting bar 40. Further, a first static electricity prevention circuit 34 may be provided between a first connection line 44 and the odd-numbered data lines DL1, DL3, ..., DL(n-3), DL (n-1). Among the data lines DL, even-numbered data lines DL2, DL4, ..., D(n-2), DLn are connected to the first shorting bar 40. Further, a second static electricity prevention circuit 36 may be provided between a second connection line 46 and the even-numbered data lines DL2, DL4, ..., D(n-2), DLn.

[0049] In this way, as illustrated in FIGs. 3 and 4, TFTs are provided at crossing areas of the gate lines GL and the data lines DL on the lower substrate 32, and pixel electrodes 72 are arranged in a matrix at pixel areas defined by the data lines DL, the gate lines GL and the common lines CL. Further, common electrodes 76, which may have a stripe shape, are

provided to form horizontal electric fields with and to be alternate with the pixel electrodes 72 at pixel areas.

[0050] The TFT includes a gate electrode 66 connected to the gate line GL, a source electrode 68 connected to the data line DL, and a drain electrode 70 connected to the pixel electrode 72 through a contact hole 74. Further, the TFT includes semiconductor layers 78 and 80 to form a conduction channel between the source electrode 68 and the drain electrode 70 by a gate voltage applied to the gate electrode 66. The semiconductor layers 78 and 80 are formed on a gate insulating film 82. Such a TFT selectively applies the data signal from the data line DL to the pixel electrode 72 in response to the gate signal from the gate line GL.

[0051] The pixel electrode 72 is located at the pixel area defined by the data lines DL and the gate lines GL, and is made from a transparent conductive material, of which the light transmittance is high. The pixel electrode 72 is formed on a protective layer 84 that is spread on the entire surface of the lower substrate 32 and is electrically connected to the drain electrode 70 through the contact hole 74 passing through the protective layer 84.

[0052] The common electrodes 76 are alternately located with the pixel electrodes 72 at the pixel areas defined by the data lines DL and the gate lines GL. The common electrode 76 is formed on the lower substrate 32 of the same metal as at least any one of the gate line GL, the data line DL and the pixel electrode 72.

[0053] In this way, the lower substrate 32 where the TFT, the pixel electrode 72, the common electrode 76 and a lower alignment film (not shown) are formed, as illustrated in FIG.

5, is facing an upper substrate 31 where a black matrix 54, a color filter 56, a planarization layer 58 and an upper alignment film (not shown) are provided.

[0054] The black matrix 54 is formed in a matrix on the upper substrate 31 to divide the surface of the upper substrate 31 into a plurality of cell areas where the color filters 56 are formed, and at the same time acts to prevent light interference between adjacent cells. Color filters 56 of the three primary colors red, green and blue are provided on the upper substrate 31 that is divided into cells by the black matrix 54. The color filters 56 are formed of acrylic or polyimide resin containing pigments and are separated from each other on the black matrix. The color filters of each color may be separately formed to prevent the colors from mixing during the fabrication process. The planarization layer 58 to planarize the upper substrate 31 is provided on the surface of the color filter 56. The planarization is to prevent the color filter 56 from being contaminated and compensates the step difference between the red, green and blue color filters 56 that are separately formed.

[0055] In the liquid crystal display device, if a gate high pulse is applied to the gate electrode 66 of the TFT, a horizontal electric field corresponding to a difference voltage between a video data voltage and a common voltage is applied between the pixel electrode 72 and the common electrode 76 for a scan period while a channel is formed between the source electrode 68 and the drain electrode 70. The horizontal electric field causes the liquid crystal of a liquid crystal layer 60 to be driven, thereby controlling the amount of incident light from a backlight.

[0056] The liquid crystal display device according to the present invention has a first bypass capacitor C1 formed at a non-display area to be connected to the end of the data line DL. The first bypass capacitor C1, as illustrated in FIG. 6A, includes a first shorting bar 40 and a first dummy line 52 formed with a gate insulating film 82 and a protective film 84 therebetween. The first bypass capacitor C1, as illustrated in FIG. 6B, includes the first shorting bar 40 formed on the gate insulating film, the first dummy line 52 overlapping the first shorting bar 40, and the protective film 84. That is, the first shorting bar 40 may be formed of the same gate metal as the gate electrode 66, and the first shorting bar 40 and the gate electrode may be formed at the same time. Or, the first shorting bar 40 may be formed of the same data metal as the source and drain electrodes 68 and 70 and the first shorting bar 40 and the source and drain electrodes 68 and 70 may be formed at the same time. The first dummy line 52 may be formed of the same transparent conductive metal as the pixel electrode 72, and they may be formed simultaneously. The first dummy line 52 may be or may not be supplied with a designated electric field. Herein, the transparent conductive metal may include Indium Tin Oxide ITO, Indium Zinc Oxide IZO or Indium Tin Zinc Oxide ITZO.

[0057] If the first shorting bar 40 is formed of the gate metal, the first bypass capacitor C1 having the first shorting bar 40 and the first dummy line 52 is formed with the gate insulating film 82 and the protective film 84 therebetween. If the first shorting bar 40 is formed of the data metal, the first bypass capacitor C1 having the first shorting bar 40 and the first dummy line 52 is formed with the protective film therebetween.

[0058] The second bypass capacitor C2 is formed at the non-display area to be connected to the end of the gate line GL. The second bypass capacitor C2 having a second shorting bar 42 and a second dummy line 50 is formed with the protective film 84 or the gate insulating film 82 and the protective film 84. The second bypass capacitor C2, as illustrated in FIG. 6B, includes the second shorting bar 42 on the gate insulating film 82 and the second dummy line 50 formed to overlap the shorting bar 42 and the protective film 84, while having the shorting bar 42 and the protective film 84 therebetween. That is, the second shorting bar 42 may be formed of the same gate metal as the gate electrode 66, and the second shorting bar 42 and the gate electrode may be formed at the same time. Or, the second shorting bar 42 may be formed of the same data metal as the source and drain electrodes 68 and 70, and the second shorting bar 42 and the source and drain electrodes 68 and 70 may be formed at the same time. The second dummy line 50 is formed of the same transparent conductive metal as the pixel electrode 72, and they may be formed simultaneously. The second dummy line 50 may be or may not be supplied with a designated electric field.

[0059] If the second shorting bar 42 is formed of the gate metal, the second bypass capacitor C2 having the second shorting bar 42 and the second dummy line 50 is formed with the gate insulating film 82 and the protective film 84 therebetween. If the second shorting bar 42 is formed of the data metal, the second bypass capacitor C2 having the second shorting bar 42 and the second dummy line 50 is formed with the protective film 84 therebetween.

[0060] When there occurs an open in a bypass loop consisting of the first shorting bar 40 connected to the data lines DL, the second shorting bar 42 connected to the gate lines GL

and the common lines CL having equipotential, the first and second bypass capacitors C1 and C2 store the remaining component within the liquid crystal display panel and slowly discharge the stored remaining component. In this way, even when the bypass loop is opened, DC components or power off signals remaining within the liquid crystal display panel is stored at the first and second bypass capacitors C1 and C2, thereby minimizing the damage of the liquid crystal display panel to improve picture quality.

[0061] As described above, the liquid crystal display device according to the present invention has the bypass capacitor formed to eliminate the remaining DC components caused by poor contact between the signal lines or the open of the bypass loop within the liquid crystal display panel. The bypass capacitor is realized with the shorting bar and the dummy line formed with the gate insulating film and/or the protective film therebetween. Since the bypass capacitor stores up the remaining DC component, it may be possible to prevent the picture quality deterioration at the display area of the liquid crystal display panel, which was caused by the remaining DC component.

[0062] It will be apparent to those skilled in the art that various modification and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.